WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a group of capacitors located at least partially in an insulating layer, each capacitor comprising a bottom electrode, a dielectric layer, and a top electrode,

wherein at least part of the dielectric layer is located between the bottom and top electrodes,

wherein the bottom electrode is formed in a cup-shaped opening, the cup-shaped opening being formed in the insulating layer, and

wherein the dielectric layer and the top electrode are formed over the bottom electrode in the cup-shaped opening;

a trench formed in the insulating layer, wherein the trench connects between and crosses each of the capacitors in the group, wherein the trench forms a recess in the bottom electrode where the trench crosses the bottom electrode; and

a conductive material formed in the trench, wherein the conductive material electrically connects the top electrodes of the capacitors in the group.

2. The semiconductor device of claim 1, wherein the conductive material is formed from material of the top electrode when the top electrode material is formed.

3. The semiconductor device of claim 1, wherein the cup-shaped opening has a generally oval cross-section shape.

4. The semiconductor device of claim 1, wherein the cup-shaped opening has a round cross-section shape.

5. The semiconductor device of claim 1, wherein the cup-shaped opening has a generally rectangular cross-section shape.

6. The semiconductor device of claim 1, wherein the trench has a curved shape.

7. The semiconductor device of claim 1, wherein the trench has a generally rectangular cross-section shape.

8. The semiconductor device of claim 1, wherein the trench has a generally rounded-bottom cross-section shape.

9. The semiconductor device of claim 1, wherein the group of capacitors are storage capacitors forming parts of embedded dynamic random access memory cells on a chip that also includes a logic circuit region.

10. A method of fabricating a semiconductor device, comprising:

providing an intermediate structure having an insulating layer formed on top;

forming a group of cup-shaped openings in the insulating layer;

depositing a first conducting material over the structure such that the first conducting material substantially coats the inside of the cup-shaped openings;

removing excess portions of the first conducting material from a top surface of the structure;

forming a trench in the insulating layer, wherein the trench extends between the cup-shaped openings of the group and crosses each of the cup-shaped openings of the group, and wherein the trench forms a recess in the first conducting material where the trench crosses the cup-shaped openings;

depositing a dielectric material over the structure such that the dielectric material substantially coats the inside of the trench and substantially coats exposed surfaces of the first conducting material;

depositing a second conducting material over the structure such that the second conducting material substantially coats the inside of the trench and substantially coats the exposed surfaces of the dielectric material; and

removing excess portions of the second conducting material from a top surface of the structure.

11. The method of claim 10, wherein the semiconductor device includes dynamic random access memory cells having storage capacitors formed at the cup-shaped openings.

12. The method of claim 10, wherein the semiconductor device includes a logic circuit region and an embedded dynamic random access memory region, wherein the embedded dynamic random access memory region includes storage capacitors formed at the cup-shaped openings.

13. The method of claim 10, wherein the cup-shaped opening has a generally oval cross-section shape.

14. The method of claim 10, wherein the cup-shaped opening has a round cross-section shape.

15. The method of claim 10, wherein the cup-shaped opening has a generally rectangular cross-section shape.

16. The method of claim 10, wherein the trench has a curved shape.

17. The method of claim 10, wherein the trench has a generally rectangular cross-section shape.

18. The method of claim 10, wherein the trench has a generally rounded-bottom cross-section shape.

19. A semiconductor device, comprising:

a group of capacitors located at least partially in an insulating layer, each capacitor comprising a first conductive material layer, a dielectric layer, and a second conductive material layer,

wherein at least part of the dielectric layer is located between the first and second conductive material layers, and

wherein the first conductive material layer coats an inside surface of a cup-shaped opening, the cup-shaped opening being formed in the insulating layer; and

a trench formed in the insulating layer, wherein the trench extends between and crosses each of the capacitors in the group, wherein the trench forms a recess in the first conductive material layer where the trench crosses the first conductive material layer at the capacitors,

wherein the dielectric layer and the second conductive material layer are formed over the first conductive material layer in the cup-shaped openings and over an inside surface of the trench, such that the second conductive material layer extends between the capacitors of the group via the trench, and such that the second conductive material layer forms top electrodes for the capacitors of the group.